

ABSTRACT OF THE DISCLOSURE

A variable loop bandwidth phase locked loop in which, upon input of a succession of signals "1", no modulated signal degradation occurs and even at a high symbol rate, 5 the reference signal frequency remains low and the sampling frequencies of a phase-frequency detector and a sigma delta circuit remain low. The phase locked loop comprises: a first modulator which transforms baseband signal TX_DATA into an integer signal for specifying a division number and sends 10 it to a control terminal of a programmable divider; a second modulator which shapes an incoming baseband signal into a prescribed signal waveform and sends it to a voltage controlled oscillator; and a variable current charge pump which changes the loop bandwidth of the phase locked loop 15 according to control signal CUR.